What is claimed is:

1. A method for producing a semiconductor device having and using an alignment mark, the method comprising:

forming a first dielectric layer;

etching a trench having predetermined dimensions into the dielectric layer;

depositing a first layer of metal into the trench;

forming a second dielectric layer over the first dielectric layer and over the first layer of metal;

etching, simultaneously, channels and an opening into the second dielectric layer, at least one of the channels used as a via extending to the first layer of metal and the opening extending through the second dielectric layer whereby a bottom surface of the opening is coplanar to a top surface of the first metal layer;

filling the channels and the opening with a metal and plating a remaining portion of the surface of the second dielectric layer with metal, the filling step controlled to fill the channels and under fill the opening;

performing chemical mechanical polishing of the metal; and

depositing a non-transparent stack of layers onto the metal and the remaining portions of a top surface of the second dielectric layer, whereby the non-transparent stack of layers conforms to the surface of the under filled opening, resulting in an alignment mark on the non-transparent stack of layers.

2. The method of Claim 1 wherein the semiconductor device is a Magnetoresistive Random Access Memory.

3. The method of Claim 1 wherein the semiconductor device is a metal-insulator-metal capacitor.

4. The method of Claim 1 wherein the formation of the first and second dielectric layers is performed through chemical vapor deposition.

5. The method of Claim 4 wherein the chemical vapor deposition is plasma enhanced chemical vapor deposition.

6. The method of Claim 1 wherein the etching of the trench, channels and opening is performed through Reactive Ion Etching.

7. The method of Claim 1 wherein the first and second dielectric layers are comprised of a low constant dielectric material.

8. The method of Claim 7 wherein the low constant dielectric material is chosen from the group consisting of silk, fluorinated oxide, and silicon dioxide.

9. The method of Claim 1 wherein the metal used for filling and plating is comprised of copper.

10. The method of Claim 1 wherein the step of filling comprises:

depositing a liner layer into the channels and opening; and

depositing a metal onto the liner layer.

11. The method of Claim 10 wherein the liner layer is comprised of tantelum.

12. The method of Claim 10 wherein the liner layer is comprised of tungsten nitride.

13. The method of Claim 1 wherein the plating metal thickness is about 7500 to about 8500 angstroms.

14. The method of Claim 1 wherein etching channels and the opening into the second dielectric layer comprises:

etching a first line in the second dielectric layer to a depth that is less than the depth of the top surface of the first metal layer; and

etching a second line in the second dielectric layer to a depth coplanar to the top surface of the first metal layer while simultaneously etching the opening.

15. The method of claim 14 wherein the step of etching the second line comprises etching the second line in the same location as the first line whereby the second line effectively extends the first line for use as a via.

16. The method of Claim 1 wherein the width of the opening is greater than two times the depth of the opening.

17. A semiconductor structure comprising:

a substrate;

a first metal layer formed in the substrate, the first metal layer having a top surface at a distance x below a top of the structure;

a second metal layer formed in the substrate, the second metal layer extending from the top of the structure to a distance y below the top of the structure, the distance y less than the distance x;

a via formed in the substrate connecting the first metal layer and the second metal layer;

an alignment mark formed in the substrate extending from the top of the structure to a depth of at least x; and

a non-transparent stack layer above the second metal layer, via, and alignment mark, the stack layer conforming to the shape of the alignment mark whereby the alignment mark is visibly recognizable.

18. The structure of Claim 17 wherein the width of the alignment mark is greater than two times the depth of the alignment mark.

19. The structure of Claim 17 wherein the first and second metal layers and the via are comprised of copper.

20. The structure of Claim 19 wherein a liner is formed between the substrate and the first and second metal layers, via, and alignment mark.

21. The structure of Claim 20 wherein the liner is comprised of material selected from the group consisting of tantalum, tantalum nitride, tungsten, titanium, and titanium nitride.